# ICT Call 11 – Objective 3.1
## Nanoelectronics


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# Presentation Outline

- What are we looking for?
- Is this new?
- What do we not want?
- Additional/background documents

# ICT WP 2013 – Some information

*The Work Programme will define the priorities for calls for proposals that will result in projects to be launched in 2013.*

- ✓ *Last WP for FP7*
- ✓ *Only one year of duration*
- ✓ *It will ensure a certain degree of continuity in priorities and at the same time serve as a bridge to activities in Horizon 2020.*

# Objective 3.1 - Introduction

- *Overcoming serious barriers, which are currently slowing down the expected evolution of CMOS, including the fundamental limits of devices and materials, system level limits, energy-efficiency, power density issues, design complexity issues, and cost.*
- *In line with the ITRS roadmap.*
- *It complements **FET** ← **Obj. 3.1** → **ENIAC JU**.*
- *Take-up actions in nanoelectronics, including Europractice-type actions, are addressed under Objective 3.3.*

# Objective 3.1 - Overall aim

To reinforce European industrial leadership in Nanoelectronics as a key enabling technology through miniaturisation, energy-efficiency, performance increase and manufacturability, for information and communication systems and other applications in 2020 and beyond;

*To promote inter-disciplinary R&I activities by bringing together different research domains and constituencies with the aim of increasing impact and of bridging to Horizon 2020.*

# Objective 3.1 - Summary

Call 11

18.09.2012 - 16.04.2013

**32 M€**

| Target outcomes | Funding | |
|---|---|---|
| **a) Integration of advanced nanoelectronics devices and technologies (16nm and below)** | STREP | 31,5 M€ |
| **b) Advanced nanoelectronics manufacturing processes.** | | |
| **c) Design, modelling and simulation for advanced nano-electronics technologies** | | |
| **d) International Co-operation** | 1 SA | 0,5 M€ |

# Objective 3.1 - Target outcomes

## *a) Integration of advanced nanoelectronics devices and technologies (16nm and below)*

- *New solutions to boost performance in More Moore. This includes Ge, III-V compound semiconductors, graphene, CNT or nanowires.*
  - ✓ "Equivalent scaling"
  - ✓ Fully Depleted SoI are included
  - ✓ Memories are not excluded, but it is not our priority

- *Innovative solutions to boost functionality in More than Moore.*
  - ✓ e.g. graphene for analog/RF, new materials for high power devices

# Objective 3.1 - Target outcomes

## *a) Integration of advanced nanoelectronics devices and technologies (16nm and below)*

- *New switches for Beyond CMOS and beyond silicon, charge-based or non-charge-based with a sufficient level of technological maturity.*
  - ✓ In line with ITRS: Non-Conventional FETs and other Charge-based Information Carrier Devices (Spin FET and Spin MOSFET Transistors)
  - ✓ Non-FET, Non Charge-based 'Beyond CMOS' Devices (with certain degree of maturity)
- *Interconnects and 3D integration at device, chip and wafer level.*
  - ✓ Novel materials for interconnects
  - ✓ 3D device level: FinFets
  - ✓ 3D chip and wafer level: TSV, wafer-level packaging

# Objective 3.1 - Target outcomes

***b) Advanced nanoelectronics manufacturing processes***

- *More Moore IC Manufacturing: efficiency and productivity enhancement*
- *Manufacturing approaches to Beyond-CMOS and advanced More-than-Moore, and to their integration with nano-CMOS including 3D integration*

# Objective 3.1 - Target outcomes

## *c) Design, modelling and simulation for advanced nano-electronics technologies*

- *Circuit- and system-level modelling and simulation: e.g. quantum and atomic scale effects; electro-thermo- mechanical effects; modelling for new materials, processes and devices.*
- *Design technologies for "Si complexity" challenges addressing non-ideal scaling of device parasitics and supply/threshold voltages; manufacturing variability; thermal effects; decreased reliability; ageing effects; coupled high-frequency devices and interconnects.*
- *Innovating with nanoelectronics - designing heterogeneous SOC integration, re-using IP.*

# Objective 3.1 - Target outcomes

## *d) International Co-operation*

*One support action to develop a European strategy which addresses the challenges in manufacturing for 450 mm in dialogue with G450C and with the US, Korea, and Taiwan.*

# Is this new? Further clarifications

- *Equipment assessment in Nanoelectronics: in objective 3.3*
- *Brokerage services (EUROPRACTICE type): in objective 3.3*

# What do we not want?

- ***We want*** *very Advanced and Multidisciplinary Research, but*

- ***We do not want***
  - ***Research focused only on materials***
  - ***Research focused on large systems integration***
  - ***Duplication of R&D***
  - ***Low innovation***
  - ***Academic proposals (low exploitation, impact)***

# Additional/background documents

- ***FP7 Workshop on Advanced Nanoelectronics Technologies*** *(Sept. 2009)* ***(ftp://ftp.cordis.europa.eu/pub/fp7/ict/docs/nanoelectronics/011209-wshop-rep-ai-v7b-clean_en.pdf)***

- ***Workshop on Manufacturing of Beyond CMOS and Advanced More than Moore Devices*** *(Dec. 2010)* ***(http://cordis.europa.eu/fp7/ict/components/elements/wshop-report-v6-fin-070211.pdf)***

- ***Benefits and Measures to Set Up 450mm Semiconductor Prototyping and to Keep Semiconductor Manufacturing in Europe – Final Report*** *(Feb.2012)* ***(http://cordis.europa.eu/fp7/ict/components/documents/450mm-final-report.pdf)***

# Thank you....

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